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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/672,967	09/25/2003	Rangarajan R. Calyanakoti	42P16968	3616

7590 07/27/2006

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EXAMINER	
STEELMAN, MARY J	
ART UNIT	**PAPER NUMBER**
2191	

DATE MAILED: 07/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/672,967	CALYANAKOTI ET AL.	
	Examiner	Art Unit	
	Mary J. Steelman	2191	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *9/25/03,5/19/04*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-23 are pending.

Specification

2. The use of the trademark JAVA has been noted in this application. It should be capitalized wherever it appears and be accompanied by the generic terminology.

Although the use of trademarks is permissible in patent applications, the proprietary nature of the marks should be respected and every effort made to prevent their use in any manner which might adversely affect their validity as trademarks.

Claim Rejections - 35 USC § 101

3. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 11-14 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Claims are directed towards a machine readable medium, which as defined in the Specification at page 7, [0018] is inclusive of "propagated signals (e.g., carrier waves...". Signal claims are non-statutory, as they do not fall into one of the four categories of 35 USC 101: processes, machines, manufactures, and compositions of matter.

Claim Rejections - 35 USC § 102

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-23 are rejected under 35 U.S.C. 102(b) as being anticipated by USPN 5,274,811to Borg et al.

Per claim 1:

A method comprising:

-receiving a software program having a plurality of instructions;

-performing instrumentation on the software program to determine a plurality of addresses of the plurality of instructions of the software program in the order in which the plurality of instructions are executed by a processor.

Col. 2:55-60, 66-67 – "linking the kernel and multiple user programs, inserting calls to the appropriate trace routines so that all memory and instruction references in the execution of the link software are accurately recorded in a designated trace buffer", "link time code modification to instrument the code which is to be executed"

Per claim 2:

-inserting an instrumentation source block (ISB) before one or more instructions of the plurality of instructions to determine one or more address of the one or more instructions in the software program.

Col. 3:5-8, "linker inserts a very short stylized subroutine (ISB) call to a routine that logs the reference in a large trace buffer", col. 6:63-64, "The trace code for basic blocks inserts the instruction address (determine one or more address of the one or more instructions) as well as the size of the basic block."

Per claim 3:

-providing an offset to the ISB to remove a skew in the one or more addresses caused by performing instrumentation on the software program.

Col. 3: 29-32, "The data recorded represents the instruction of data addresses which would have been accessed had the code not been expanded with the calls", col. 7: 40-44, "linker computer the actual virtual address (or physical address for the kernel) from the base and offset data made available..." Calculations remove the skew.

Per claim 4:

-inserting a plurality of store instructions before the ISB to store content of a plurality of registers of the processor and a plurality of restore instructions after the ISB to restore the content of the plurality of registers of the processor.

Col. 10: 61-64, "The kernel uses a separate register set from user processes. To assure that the trace registers are always correct, some of their values must be copied back and forth (store / restore contents of a plurality of registers) between register sets when moving between the user and kernel modes."

Per claim 5:

-the plurality of instructions in the software program are discretely identifiable.

See FIG. 3, #44-object file (discretely identifiable).

Per claim 6:

-one or more of the plurality of instructions in the software program are not discretely identifiable.

See FIG. 3, #42-source file (not discretely identifiable).

Per claim 7:

-converting the software program into a format where the plurality of instructions are discretely identifiable.

See FIG. 3, #42 source files compiled (converted) to #44-object file (discretely identifiable).

Per claim 8:

-the ISB includes instructions to output one or more instruction addresses.

Col. 3: 26-32, "When executed, the trace routine records an instruction or data reference...The data recorded represents the instruction...addresses (output instruction addresses) which would have been accessed had the code not been expanded with the calls."

Per claim 9:

-the ISB includes a branch instruction to branch to a routine which comprises one or more instructions to output one or more of the plurality of addresses.

FIG. 5 and related text beginning at col. 7, line 4. Col. 7: 9-12, "linker is to insert fast calls (branch to routine) 64 to INSTR TRACE 66 before each basic block, to LOAD TRACE 68 before each load, and to STORE TRACE 70 before each store." The linker (col. 7: 59-67)

calculates the address of the instruction, considering an offset and loads the address into a trace buffer. Col. 8: 43-47- An analysis program analyzes the data stored in the trace buffer and stores the results of the analysis.

Per claim 10:

-appending a binary file of the output routine to a plurality of binary files of the software program;

-providing the plurality of binary files of the software program with the binary file of the output routine to a linker.

See FIG. 3, #46- link to form instrumented object module #50, FIGs. 4A, 4B, 4C- expansion of instrumented code, FIG. 5, #102-return modified object module to system linker (providing binary files with binary file of output / instrumentation routine to a linker) after inserting instrumentation and correcting for offsets.

Per claim 11:

A machine-readable medium embodying codes, the codes, when executed by a processor, causing the processor to perform a plurality of operations, the plurality of operations comprising: receiving a software program having a plurality of instructions; and performing instrumentation on the software program to determine a plurality of addresses of the plurality of instructions of the software program in the order in which the plurality of instructions are executed by a processor.

This is a 'machine-readable medium' version of claim 1. See rejection of limitations addressed in claim 1 above.

Per claim 12:

-performing instrumentation on the software program comprises inserting an instrumentation source block (ISB) before one or more instructions of the plurality of instructions to determine one or more address of the one or more instructions in the software program.

See rejection of limitations addressed in claim 2 above.

Per claim 13:

- performing instrumentation on the software program further comprises providing an offset to the ISB to remove a skew in the one or more address caused by instrumentation of the software program.

See rejection of limitations addressed in claim 3 above.

Per claim 14:

-instrumentation of the software program further comprises inserting a plurality of store instructions before the ISB to store content of a plurality of registers of the processor and a plurality of restore instructions after the ISB to restore the content of the plurality of registers of the processor.

See rejection of limitations addressed in claim 4 above.

Per claim 15:

A system comprising: a processor; and a dynamic random access memory ("DRAM") device to store a first computer program, the first computer program including a first plurality of instructions, which when executed by a processor, causes the processor to perform a plurality of operations on a second computer program, the plurality of operations comprising receiving the second computer program, the second computer program having a second plurality of instructions; and performing instrumentation on the second computer program to determine a plurality of addresses of the second plurality of instructions of the second computer program in the order in which the second plurality of instructions are executed by the processor.
This is a 'system' version of claim 1. See rejection of limitations addressed in claim 1 above.
A first computer program references the instrumented monitoring code. A second computer program references the program to be monitored.

Per claim 16:

-performing instrumentation on the second computer program comprises inserting an instrumentation source block (ISB) before one or more instruction of the second plurality of instructions to determine one or more address of the one or more instruction in the second computer program.
See rejection of limitations addressed in claim 2 above.

Per claim 17:

-performing instrumentation on the second computer program further comprises providing an

offset to the ISB to remove a skew in the one or more address caused by performing instrumentation on the second computer program.

See rejection of limitations addressed in claim 3 above.

Per claim 18:

-performing instrumentation on the second computer program further comprises inserting a plurality of store instructions before the ISB to store content of a plurality of registers of the processor and a plurality of restore instructions after the ISB to restore the content of the plurality of registers of the processor.

See rejection of limitations addressed in claim 4 above.

Per claim 19:

-the second plurality of instructions in the second computer are discretely identifiable.

See rejection of limitations addressed in claim 5 above.

Per claim 20:

-the second plurality of instructions in the second computer program are not discretely identifiable.

See rejection of limitations addressed in claim 6 above.

Per claim 21:

-the plurality of operations comprises converting the second computer program into a format in

which the second plurality of instructions are discretely identifiable.

See rejection of limitations addressed in claim 7 above.

22. The system of claim 16, wherein the ISB includes instructions to output the one or more address of the one or more instruction in the second computer program.

See rejection of claim 8 above.

23. The system of claim 16, wherein the ISB includes a branch instruction to branch to a routine which includes one or more instructions to output the one or more address of the one or more instruction in the second computer program.

See rejection of claim 9 above.

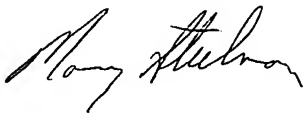
Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mary Steelman, whose telephone number is (571) 272-3704. The examiner can normally be reached Monday through Thursday, from 7:00 AM to 5:30 PM If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wei Zhen can be reached at (571) 272-3708. The fax phone number for the organization where this application or proceeding is assigned: 571-273-8300.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mary Steelman 

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